Microwave Journal

Ku-band MMIC Power Amplifiers Developed Using MSAG MESFET Technology

This article presents the design approach and test results of 1, 1.5, 2 and 5 W, Ku-band MMIC power amplifiers developed using the high performance MSAG MESFET technology. Both single-ended and balanced topologies were used. A minimum power-added efficiency (PAE) of 27 percent, an output power (P_{out}) of 5 W and an associated gain of 21.5 dB were achieved over the 12.5 to 14.5 GHz frequency range. To the author's best knowledge, these results represent the state-of-the-art in MESFET-based MMIC Ku-band power amplifiers.

TABLE I

SUMMARY OF Ku-BAND REACTIVELY MATCHED MEDIUM POWER AMPLIFIERS

Frequency Range (GHz)	No. of Stages	Gain (dB)	P_o (W)	PAE (%)	Device Technology	Year Reference
8 to 13.5	2	–	2.5	38	0.2 µm pHEMT	1996[1]
8 to 14	2	15	2.8	36	HBT	1998[2]
13 to 15.0	2	–	6.0	–	0.15 µm pHEMT	2002[3]
Ku/K	3	22	6.0	30	0.25 µm pHEMT	2003[4]
13.5 to 15	3	22	8.0	22	0.25 µm pHEMT	2004[5]
14.0 to 14.5	2	15	1.8	22	0.25 µm pHEMT	2004[6]
12.5 to 14.5	3	19	7.0	27	0.4 µm MESFET	this work

During the past decade, there has been significant progress in monolithic Ku-band power amplifiers operating over both narrow and broad bands. Many different technologies, including MESFET, HBT and HEMT, are being pursued to develop MMIC power amplifiers[1–6] in order to obtain the maximum output power (P_{out}) and power-added efficiency (PAE) from a single chip. Progress in this area, for Ku-band MMIC power amplifiers, has been summarized in ***Table 1***. The performance listed is the minimum over the frequency range. MMICs with greater than 1 W output power were selected for comparison. The gain shown is taken at the minimum power level. Although MIC technology can be used to develop broadband power amplifiers, power MMIC amplifiers, in general, offer smaller size and lightweight, higher gain, wider bandwidth, higher reliability, lower cost and much better unit-to-unit amplitude and phase tracking capability, when manufactured in large volume. MMIC power amplifiers have the following potential advantages as compared to commonly available internally matched power amplifiers:

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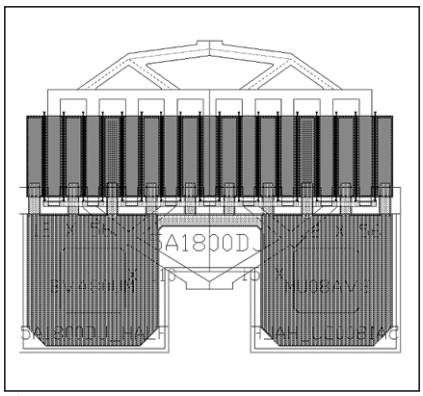


▲ *Fig. 1 Physical layout of the 1.8 mm FET with offset vias.*

- Multistage designs have higher gain (20 to 30 dB)
- Higher overall power-added efficiency (PAE)
- Compact in size and lightweight
- Lower parts count, higher reliability and lower cost
- No external biasing chokes are required

Several high efficiency C- and X-band power MMIC amplifiers have been developed successfully using the high performance, low cost and highly reliable multifunction self-aligned gate (MSAG) MESFET IC process[7–16] at the M/A-COM facility in Roanoke, VA. These amplifiers have demonstrated PAEs in excess of 55 and 40 percent with associated output powers of 14 and 12 W, at C- and X-band, respectively, over approximately a 15 percent bandwidth.[12,13] These results represent the state-of-the-art power amplifier performance at C- and X-band and the MSAG MESFET technology provides a low cost solution to the power section of active aperture phased-array T/R modules.

In this process, the ion-implanted active devices use 0.4 µm gates, deposited by employing low cost optical lithography, leading to higher throughput and lower cost. The MSAG process has unique features: it does not use air bridges, has polyimide scratch protection, multi-level plating capability[15] for low loss passive components, no hydrogen poisoning susceptibility and is very reproducible unit to unit. These features all lead to a mean time to failure (MTTF) greater than 100 years at a channel temperature of 150°C, higher assembly yields with MSAG chips and provide cost-effective solutions.

The MSAG process also uses three layers of polyimide ($\varepsilon_r = 3.2$): interlevel dielectric (3 µm thick), inductor crossover layer (7 µm) or low loss microstrip (10 µm thick) and a scratch protection buffer layer (7 µm thick) for mechanical protection of the finished circuitry. Three metal layers are used: metal 1 (0.5 µm thick), first plated gold (4.5 µm thick) and second plated gold (4.5 µm thick). The multi-level plating (MLP) process allows a reduction in the chip size and lowers the resistive loss in passive components. Low capacitance metallization crossovers are achieved by a polyimide intermetal dielectric layer. The front side processing is completed by depositing a polyimide buffer layer. The buffer layer provides mechanical protection of the circuit structures during backside processing, dicing and subsequent assembly operations. Finally, the wafers are thinned to their final thickness of 75 µm, through-wafer vias are etched and the backside is metallized.

This article describes the design and test results of several fully monolithic, class AB, Ku-band MMIC power amplifiers, designed to operate at a nominal power supply voltage of 8 V. The amplifiers described include a high gain, high PAE and linearity 1.5 W amplifier; a broadband 1.5 W amplifier; a 2 W balanced amplifier; and a 5 W high power amplifier. The general design approaches, along with salient features of each design, are also discussed.

GENERAL DESIGN APPROACH

The MSAG MESFET technology was selected to develop Ku-band power amplifiers because of its high across-the-wafer uniformity, excellent linearity and low cost capabilities. One of the basic requirements for achieving high power output and PAE on a single MMIC chip is the high across-the-wafer uniformity of the saturated drain-source current (I_{DSS}) and device cut-off frequency (f_T) in order to combine all unit FET cells efficiently. The high across-the-wafer uniformity for efficient power combining becomes more important at higher frequencies. The MSAG transistors, based on a self-aligned gate approach, have a planar channel structure contributing to better across-the-wafer uniformity, reproducibility and manufacturability.

FET Size

The design of the MMIC power amplifier starts with the selection of the number of stages and unit FET sizes required, based on the gain, PAE/linearity and output power requirements. The choice of FET cell size impacts the matching networks, combining topology, chip size and electrical performance. Larger FET cell sizes reduce the chip area because fewer combiners are required. However, they have lower input and output impedances, which increase the impedance matching ratio of the matching networks, increasing circuit mismatch loss and reducing bandwidth. In addition, there is a reduction in the FET's performance due to increased parasitic reactances and resistances. This latter effect is minimized with careful FET design.

Except for the 5 W HPA, the unit FET's gate periphery was restricted to less than 0.8 mm. The Ku-band MMICs have demonstrated power densities of 0.6 W/mm at V_{DS} = 10 V and 0.48 W/mm at V_{DS} = 8 V, which are used to determine the total FET periphery needed in the design of these power amplifiers. This translates to eight 1.8 mm gate periphery FETs with offset vias arranged edge-to-edge creating effectively an eight-feed 14.4 mm FET to achieve 5 W output power at V_{DS} = 8 V. The large gate periphery 1.8 mm FET shown in ***Figure 1*** uses offset vias and has a lower source inductance (higher gain) than in-line via FETs of similar gate periphery. FETs with a smaller than 0.8 mm gate periphery have in-line source vias. A binary corporate feed combining, that is two FETs, driving four FETs, which finally drive eight FETs, was used to realize better linearity and to maintain good layout symmetry to obtain maximum possible performance.

After the selection of FET sizes, the FET's gate periphery, the number of fingers in each FET cell and gate-to-gate pitch are finalized. The unit gate width for each FET is the FET size or periphery, divided by the number of fingers, and is a function of device type and frequency of operation. The gate pitch determines the area over which the FET dissipates power; a larger pitch reduces the FET channel temperature. The design of the output FETs is key in re-

TABLE II

SUMMARY OF THERMAL ANALYSIS OF Ku-BAND FETs

FET Size (mm)	No. of Fingers	Gate-Gate Pitch (μm)	Thermal Resistance R_{TH} (°C/W)	Net Power Dissipated (W) Based on 0.5 W/mm	ΔT (°C)
0.3	4	30	267.9	0.15	40.2
0.625	6	30	132.2	0.313	41.3
0.625	6	20	146.8	0.313	45.9
0.75	6	30	110.2	0.375	41.3
1.80	18	24	51.0	0.90	45.9
14.4	144	24	6.5	7.2	46.8

ducing the chip area. Keeping in mind the electrical, physical and thermal design requirements for each design, appropriate physical dimensions were selected for each FET.

Thermal Design

The thermal modeling of semiconductor devices can be performed by using numerical techniques such as the finite difference and finite element analyses or by using simple analytic methods such as the Cooke model.[17] Based on published data and the measurements carried out at M/A-COM, it is believed that the Cooke model predicts FET channel temperature accurately. The first step is to calculate the thermal resistance (R_{TH}) of each FET used in the designs. The thermal resistance is calculated, based on the FET structure (gate-to-gate pitch, unit gate width and FET size) and the substrate properties. The maximum channel temperature rise can then be obtained, knowing the power dissipated in the device. ***Table 2*** summarizes the thermal resistance calculations for several FETs used in the designs. The GaAs substrate thickness and thermal conductivity at room temperature are 75 μm and 0.46 W/cm°C, respectively. The difference in the temperature, ΔT, from the bottom surface (carrier) to the top surface (channel) of the MMIC chip is calculated using $\Delta T = R_{TH} \times P_{DC}$, where P_{DC} is the net power dissipated in the device. For these calculations, the thermal resistance goal is chosen based on the maximum allowed junction temperature of 150°C.

Consider a FET having a 100 μm unit gate width and a 24 μm gate-to-gate spacing. According to Cooke's model, the incremental increase in R_{TH} value per unit width of a FET from fingers 1 to 2, 2 to 4, 4 to 18 and 18 to 144 fingers is 19, 14, 9 and 2 percent, respectively. This means that the R_{TH} value for closely spaced heat sources is about 45 percent higher than the isolated heat source. Thus, any physical separation between the FETs helps in lowering the R_{TH} value. In the Ku-band amplifiers, all FETs are isolated, except the 1.8 mm FET used in the output stage of the 5 W HPA. In the 5 W HPA, the output stage eight FETs are treated as one FET of 14.4 mm gate periphery for thermal resistance calculations.

The next step is to calculate the net power dissipation in the FETs under RF drive. An in-house program was used to calculate the power delivered to each FET and the power delivered out of each FET in order to calculate the net power dissipated in the devices. Based on these calculations and the measured hybrid FET performance data, an average value of 0.5 W/mm power dissipation was used to calculate the value of ΔT for each FET.

Load Impedance

A unit cell of 625 μm FET was characterized at 10 V and 14 GHz using a load pull technique. The measured load for this FET is equivalent to the parallel combination of a 90 Ω resistor (R_L) and a –0.10 pF capacitor (C_L). In the design, for other FET peripheries, the load impedance was obtained by using the following scaling relationships

$$R_L = \frac{90 \times 0.625 \times V_{DS}}{Wg \times 10}\ \Omega \qquad (1)$$

$$C_L = -\frac{0.19 \times Wg}{0.625}\ pF \qquad (2)$$

where

Wg = total FET periphery in mm
V_{DS} = operating drain voltage in volts

TABLE III

SUMMARY OF MEASURED PERFORMANCE AT 14.5 GHz OF A 0.625 MSAG FET BIASED FOR CLASS AB OPERATION

Parameter	Value @10 V	Value @8 V
Power gain (dB)	8.4	8.5
Power output (dBm)	27	26
PAE (%)	60	62
V_{GS} (V)	–2	–1.8

As a first-order approximation, the reactive part of the load is assumed to be independent of the drain voltage. The negative sign in Equation 2 represents an inductive reactance. For example, for a 1 mm FET, operating at 8 V, the values of R_L and C_L are

$$R_L = 45\ \Omega$$
$$C_L = -0.304\ pF$$

This scaling method for obtaining the load impedance works reasonably well for a 6 to 10 V operation, for gate peripheries less than 3 mm and up to 20 GHz, when the FET's output feed is designed or scaled accordingly.

Hybrid amplifiers at 14.5 GHz were designed using the aforementioned load pull data. Typical measured performance obtained for the 0.625 mm FET biased at 10 V and 20 to 30 percent I_{DSS} is shown in ***Table 3***.

Linear and Nonlinear Models

The design of Ku-band amplifiers was based on both the linear and nonlinear MSAG FET models. For linear simulations, equivalent circuit (EC) models and small-signal S-parameters obtained over 0.5 to 40 GHz at the operating bias point were used. The EC model topology used is typical of most FET models in the commercial simulators. The Q-point of the FETs was selected for class AB operation (approximately 30 percent I_{DSS}) of the device, in order to obtain the maximum P_{out}, PAE and linearity. Four sets of S-parameter data, corresponding to device low gain, high gain, low current and high current, were used in the amplifier designs.

The nonlinear FET model used to simulate the Ku-band amplifiers is based on a modified Materka model,[18] optimized to predict accurately the output power and PAE. The nonlinear model has I-V equations along

TABLE IV

SIMULATED DATA FOR SEVERAL MSAG FETs USING NONLINEAR MODELS AT 12 GHz, BIASED AT 10 V

FET Size (mm)	Gate-Gate Pitch (μm)	No. of Fingers	G_{max} (dB)	P_o (dBm)	G_A (dB)	PAE (%)
0.625	30	6	13.8	27.1	9.5	64
0.94	30	10	13.4	28.5	9.3	60
1.50	30	14	12.5	30.6	8.4	58
1.8	24	18	11.5	31.5	8.0	57
2.50	20	24	10.4	32.7	7.5	55

with improved capacitance equations compiled into a commercial CAD tool. The model parameters were extracted using extensive S-parameter data, load pull data and pulsed I-V data. The nonlinear model was verified for the standard 0.625 mm FET using extensive hybrid measurements at 14.5 GHz.

Table 4 summarizes the electrical performance of MSAG FETs at 12 GHz calculated using the nonlinear model. The device gain and PAE are reduced significantly by increasing the device size from 0.625 to 2.5 mm.

AMPLIFIER DESIGN CONSIDERATIONS

In this section, a summary of design considerations, used in the design of Ku-band power amplifiers, is described. This includes chip size, loss in matching networks, electromigration requirements and stability considerations.

Chip Size

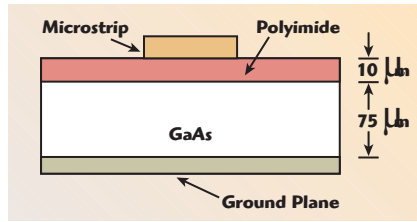
In general, larger sizes used in power amplifier MMICs perform better in terms of RF parameters and thermal design. However, reducing the chip area will be a significant cost saving requirement, provided that all other characteristics such as reliability and RF yield are almost the same. Reducing the chip area contributes to MMIC cost reduction in two ways: a larger number of chips per wafer, and higher visual and functional yields. For example, M/A-COM's yield model for MSAG processing predicts that reducing the chip area from 40 mm^2 to 20 mm^2 will improve MMIC visual and functional yields by a factor greater than 1.2. Thus, reducing the chip area of power amplifiers is an important factor to reduce their costs. An 18 mm^2 chip area was selected for the 5 W HPA to achieve a goal of better than 0.3 W/mm^2 power density at 10 V.

Low Loss Matching Networks

It is desirable to lower the dissipative loss in the power amplifier's output matching network (using lumped inductors and microstrip lines) in order to improve the P_{out} and PAE performance. The dissipation loss in the microstrip matching networks was improved by using the modified microstrip structure shown in ***Figure 2***. This structure is compatible with MMIC fabrication using a multi-level plating (MLP) process.[15] The strip conductor is fabricated on a thin polyimide dielectric layer, which is placed on top of the GaAs substrate. This allows more of the electric flux lines in the air and thus resembles a suspended microstrip line, which has a much lower dissipation loss than a conventional microstrip. Another way to think of this is that instead of inserting 50 to 75 μm of additional GaAs beneath the line, a thinner layer of 10 μm thick polyimide (a material with lower permittivity) has been inserted in order to reduce the dissipative loss by half.[19] The impedance of such lines can be increased by 40 to 60 percent as compared to standard lines on the given base substrate. This modified structure also helps in the fabrication of the feed structure of the offset via FETs.

The additional thick metallization layer available in the MLP process offers benefits as well, mostly in the area of DC current routing/high power design and extending the usage of passive components to lower frequencies. Most straightforwardly, the designer now has the flexibility to use 9 μm thick transmission lines. The current handling for such lines is 20 mA/μm.[20–22]

A second benefit of the additional thick metal layer is the option to create high current structures, such as spiral inductors. Previously, spiral inductors could be current limited, based on the width of the thin metallization underpass to get from the center of the spiral, typically 2 mA/μm as compared to 10 mA/μm for 4.5 μm thick lines. With MLP, a spiral inductor can be fabricated with 4.5 μm thick spirals and 4.5 μm thick underpasses.



▲ *Fig. 2 Multilayer microstrip configuration.*

In this design, low loss microstrip lines on a 10 μm thick polyimide layer[19] are used to lower the loss, especially in the output matching network. Since the lines on polyimide have poor thermal conductivity, a thermal design for such lines is also performed.[23,24]

Electromigration Requirements

Electromigration requirements dictate the microstrip and inductor line widths carrying DC current. A conservative current density of 2.2×10^5 A/cm^2 is used as an electromigration limit for the 4.5 μm thick gold conductors. This translates to a maximum allowed current per unit line width of 10 mA/μm. The maximum current expected in the output FET for this design is approximately 2A. This dictates that, in the output matching network, dual drain bias lines should be used, and each line must be 100 μm wide. The requirement for such wide, low impedance shunt lines complicates efforts to shrink the chip area, and also gives rise to unbalance in the output feed lines due to junction discontinuity effects, impacting significantly the circuit bandwidth. Compact lumped elements are used in the earlier stages where power and current densities are less.

Stability

For MSAG FETs, the experience has been that the standard even mode ($K > 1$) and odd mode stability analyses are adequate to avoid mi-

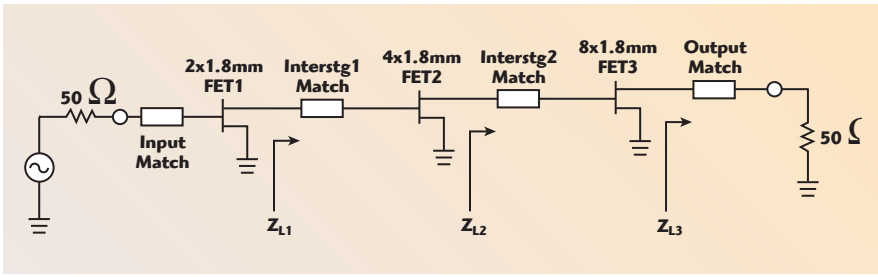


Fig. 3 Three-stage power amplifier configuration depicting the load required at the drain of each FET stage.

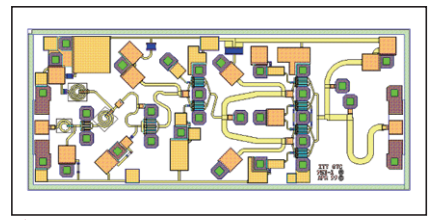


Fig. 4 Layout of the Ku-band linear power amplifier (chip size is 4.3 x 1.8 mm).

crowave oscillations. However, under a large-signal condition and pulsed operation, it is necessary to design a worst-case K-factor greater than 1, based on S-parameter data for various bias conditions from V_{DS} = 3 V and 50 percent I_{DSS} to V_{DS} = 10 V and 25 percent I_{DSS}, to ensure the amplifier's stability. This approximately replicates the envelope a full cycle of the input signal experiences during the large signal and pulsed operation. It was found that imposing a K > 2.0 condition for V_{DS} = 10 V and 25 percent I_{DSS} small-signal S-parameters is adequate to ensure unconditional stable operation under all conditions. Exercising special care in maintaining the symmetry in the amplifier's layout and properly selecting isolation resistors prevents odd mode oscillations.

Design Methodology

Traditionally, a power amplifier can be designed based on the load line method.[25–28] The design of Ku-band MMIC power amplifiers was based on a design methodology using small signal and nonlinear FET models and load pull data obtained at the operating bias point. In this method, initially, the load line technique[25,26] is used to optimize the circuit parameters. For example, in a three-stage, 5 W power amplifier, the optimum load impedances Z_{L1}, Z_{L2} and Z_{L3} at the drain of the first, second and third stage FETs, respectively, which are necessary to realize maximum output power and PAE, are shown in ***Figure 3***. Then the design is simulated using the nonlinear model to calculate the power compression of each stage and the output power and PAE as a function of input power. Since it is very difficult to realize the required load impedances over wide bandwidths and to optimize a circuit using a nonlinear model, the above design process is repeated so that an optimum solution for simultaneous match for load impedances at the drain of each FET and best gain, power and PAE are achieved.

The Ku-band amplifiers were designed using a low loss matching (LLM) design technique.[29] This technique has been successfully applied to the design of power amplifier drivers and high power amplifiers at M/A-COM's Roanoke facility. In this scheme, both the resistive or dissipative loss (DL) and mismatch loss (ML) for each stage are calculated and controlled as required in the design. Generally, DL and ML for the output match are kept at a minimum and the ML for each interstage is minimized. The controlling factors for DL and ML for each interstage include stability criteria and electrical performance. This also helps in optimizing the FET aspect ratios. The dissipative loss is for the individual passive stage, that is interstage, output, etc., and the mismatch loss is the difference between the required device's optimum load impedance and the transformed 50 Ω output impedance at the drain terminal of the FET. The previously described method is based on the assumption that the device input impedance depends strongly on the load connected at the drain terminal rather than its large-signal parameters. For FETs and HEMTs, this assumption is fairly accurate and is the cornerstone of the multistage Ku-band designs.

In the matching networks, a reactive binary matching topology was used, employing low pass and high pass networks that provide higher power output and PAE. Both lumped elements and distributed circuit elements were used for impedance matching networks. In the design optimization using the load line technique, four sets of S-parameter data, corresponding to low gain, high gain, low current and high current, were used. These data files represent the possible fabrication changes and allow a design to be realized that is more tolerant to process variations.

The input stage, which has a limited gain compensation network, was designed for good input match as well as for maximum power transfer at the high frequency end. The interstage matching networks were designed to provide a flat gain response and enough output power to the succeeding stage FETs for achieving maximum output power and PAE. The output matching elements were selected to provide an optimum load match with minimum possible insertion loss, since the efficiency is reduced to a greater extent by a given amount of loss due to decreased power out, gain and available DC power at the FET drain pads. Each stage as well as the complete amplifier were designed to be unconditionally stable over a 3 to 10 V drain power supply and 25 to 50 percent I_{DSS} drain current. EM simulations were used extensively during circuit optimization for closely packed passive circuit components and discontinuities.

HIGH GAIN, PAE/LINEARITY POWER AMPLIFIER

The four-stage design consists of a 0.3 mm, a 0.625 mm, two 0.625 mm and four 0.625 mm FETs in the first, second, third and fourth stages. All FETs have a 30 µm gate-to-gate pitch. The FET 2:1 aspect ratio maintains a better linearity. The circuit was designed for high 1 dB power compression (P1dB) and high gain. Single drain pad and single gate pad supply operations were used. The first three stages use small resistors in the drain bias lines for stabilization. The values of the resistors and their sizes were selected so that the voltage drop across them is less than 0.5 V and they also meet the electromigra-

tion requirements. In the gate bias lines, the isolation resistors values were 200 Ω per mm of FET periphery. The nominal drain supply voltage is 8 V and the gate voltage is –2 V.

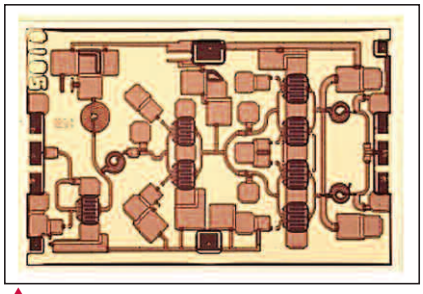


Fig. 5 Layout of the broadband power amplifier (chip size is 3.0 x 1.8 mm).

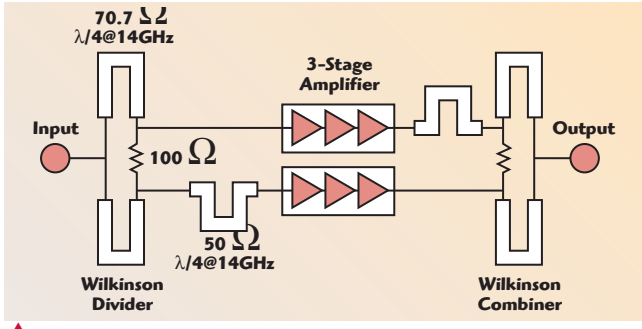


Fig. 6 2W, Ku-band, balanced power amplifier configuration.

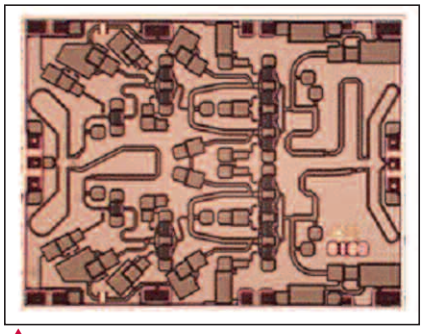


Fig. 7 Photograph of the Ku-band balanced 2W amplifier (chip size is 4.4 x 3.4 mm).

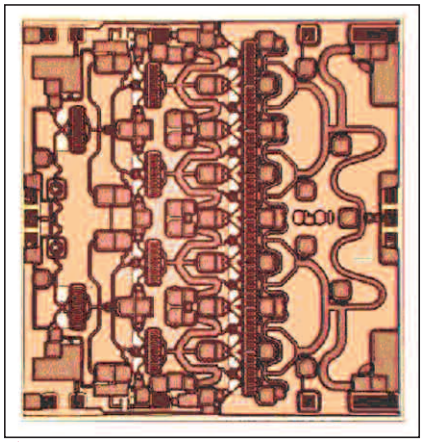


Fig. 8 Photograph of the Ku-band 5W amplifier (chip size is 4.2 x 4.4 mm).

Figure 4 shows the physical layout of the MMIC amplifier.

BROADBAND POWER AMPLIFIER

The three-stage design comprised of a 0.625 mm FET at the input driving two 0.625 mm FETs and driving four 0.625 mm FETs at the output. The FET 2:1 aspect ratio, in this case, is required to obtain high power and PAE over a larger bandwidth. This design also uses a single drain pad and single gate pad supply operation. ***Figure 5*** shows the layout of the three-stage broadband amplifier.

BALANCED 2 W POWER AMPLIFIER

The 2 W power amplifier uses a balanced configuration, as shown in ***Figure 6***. In this design, Wilkinson divider/combiners with 90° phase offset 50 Ω lines were used instead of Lange couplers. In this case, the reflected signals from the two single-ended amplifiers have a 180° phase difference across the 100 Ω isolation resistor. Thus, the out-of-phase reflected signals are absorbed in the isolation resistor. This topology minimizes the reflected signals at both the input and output terminals and provides good VSWR. Also, the effect of mismatch on the output power and PAE, due to bond wires and package lead frame, is minimum.

The single-ended amplifier's FET topology is the same as for the broadband amplifier using a 2:1 FET aspect ratio. This design requires a bias supply from both sides. ***Figure 7*** shows a photograph of the balanced 2 W amplifier.

5 W HPA

The 5 W HPA design uses two 1.8 mm FETs driving four 1.8 mm FETs and driving eight 1.8 mm FETs. Here, the FET aspect ratio is 2:1 and the circuit is designed for maximum P_{out} and PAE under saturation. The matching circuit microstrip lines are on 10 µm polyimide. ***Figure 8*** shows a photograph of the 5 W MMIC HPA. This design requires a bias supply from both sides.

TEST DATA FOR THE KU-BAND MMIC CHIPS

Several MMIC amplifier chips for each design were assembled on gold-plated Elkonite (Cu-W alloy) carriers for RF characterization after "on-wafer" pulsed power screening. The Elkonite material was chosen for its good thermal conductivity and good thermal expansion match to GaAs and alumina. The ICs were die attached on a pedestal, using gold-tin (AuSn) at 300°C, in order to keep the bond wire lengths to a minimum be-

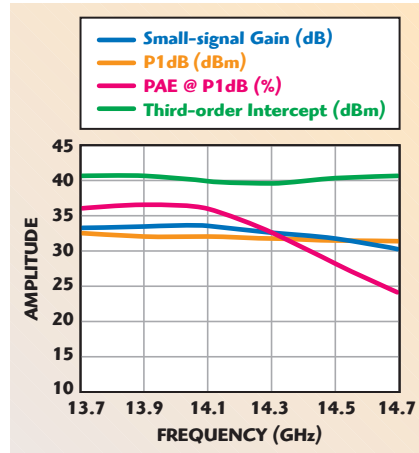


Fig. 9 Typical measured gain, P1dB, PAE and output third-order intercept versus frequency.

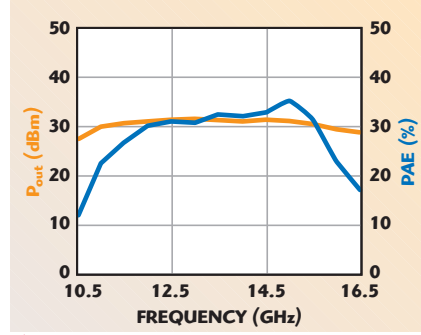


Fig. 10 Output power and power-added efficiency vs. frequency at V_{DD} = 8V and P_{in} = 18 dBm.

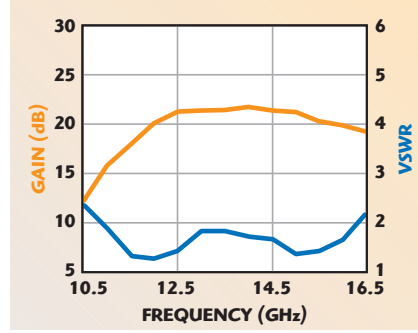


Fig. 11 Small-signal gain and VSWR vs. frequency at V_{DD} = 8V.

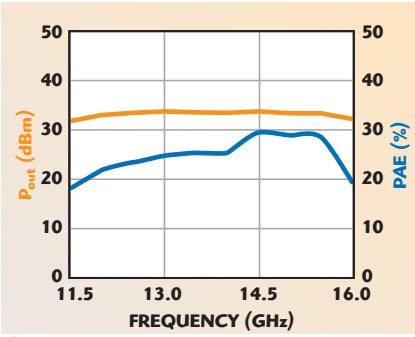


Fig. 12 Output power and power-added efficiency vs. frequency at V_{DD} = 8V and P_{in} = 18 dBm.

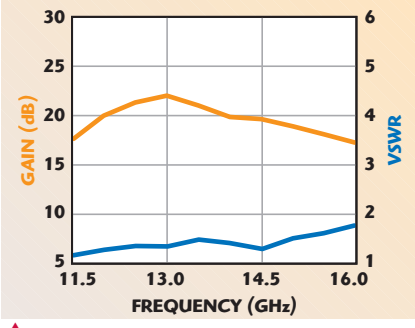


Fig. 13 Small-signal gain and input VSWR vs. frequency at V_{DD} = 8V.

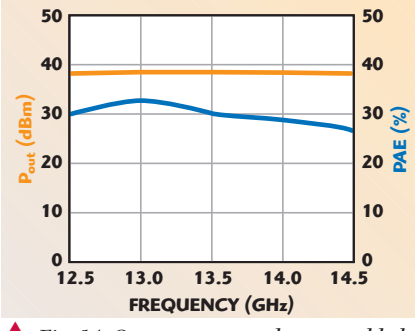


Fig. 14 Output power and power-added efficiency vs. frequency at V_{DD} = 8V and P_{in} = 23 dBm.

tween the chip and the input and output microstrip feed lines, which were printed on 15-mil thick alumina substrates. The test fixtures were fitted with high performance microstrip-to-coaxial connectors having return loss better than 20 dB up to 18 GHz. All chips were tested under CW conditions.

High Gain, PAE/Linearity Power Amplifier

The average measured performance of the four-stage linear power amplifier at V_{DS} = 8 V is shown in ***Figure 9***. The gain was approximately 32.5 ±1 dB over the 14 to 14.5 GHz frequency range. At P1dB the output power was greater than 31.5 dBm and the PAE greater than 28 percent. The output third-order intercept point (TOI) was greater than 39.5 dBm. The noise figure and second harmonic levels were also measured. Their values were less than 5 dB and -48 dBc, respectively.

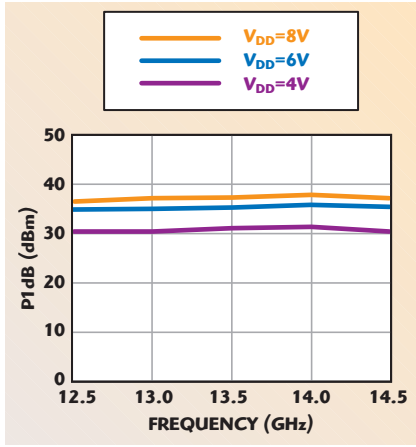


Fig. 15 1 dB compression point vs. drain voltage.

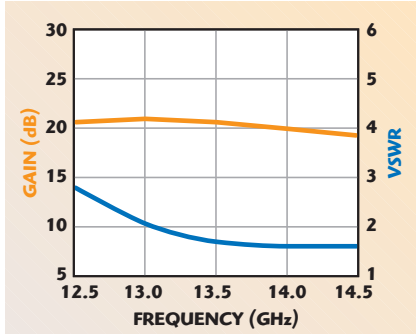


Fig. 16 Small-signal gain and input VSWR vs. frequency at V_{DD} = 8V.

Broadband Power Amplifier

The typical measured P_{out} and PAE for the three-stage broadband amplifier MMIC at V_{DS} = 8 V and P_{in} = 18 dBm are shown in ***Figure 10***. The amplifier has an output power greater than 31 dBm and a PAE better than 30 percent, over the 12 to 15.5 GHz frequency range. Over 11 to 16 GHz, the output power was better than 30 dBm. The output power was increased to 32 dBm at V_{DS} = 10 V. The variations of small-signal gain and input VSWR as a function of frequency are shown in ***Figure 11***. The input VSWR is better than 2:1 over the 10.9 to 16.4 GHz range.

Balanced 2 W Power Amplifier

Figure 12 shows the typical measured P_{out} and PAE for the balanced amplifier MMIC at V_{DS} = 8 V and P_{in} = 18 dBm. The amplifier has an output power greater than 33 dBm and a PAE better than 22 percent over the 12 to 15.5 GHz frequency range. When the supply voltage was increased to 10 V, the output power was better than 34.5 dBm. ***Figure 13*** shows the small-signal gain and input VSWR versus frequency. The input VSWR is better than 1.5:1 over the 11.5 to 15 GHz range.

5 W HPA

The typical measured P_{out} and PAE for the 5 W amplifier MMIC at V_{DS} = 8 V and P_{in} = 23 dBm are shown in ***Figure 14***. The amplifier has an output power greater than 38.5 dBm and a PAE better than 27 percent over the 12.5 to 14.5 GHz frequency range. ***Figure 15*** depicts the P1dB power levels at various drain voltages. The variations of small-signal gain and input VSWR as a function of frequency are shown in ***Figure 16***. The input VSWR is better than 2:1 over the 13.1 to 14.8 GHz range. The measured second- and third-harmonic power levels at V_{DS} = 8 V and P_{in} = 23 dBm were below –40 and –75 dBc, respectively.

CONCLUSION

A variety of Ku-band power amplifier MMICs has been developed using M/A-COM's MSAG MESFET technology. The power amplifiers have demonstrated excellent power performance: greater than 5 W output power with power-added efficiency of 32 percent at 13 GHz for the 5 W amplifier, and an outstanding PAE (36 percent) and linearity (TOI = 40 dBm) at P1dB compression and 14 GHz for the 1.5 W amplifier. This outstanding power performance was only possible because of high across-wafer uniformity of saturated drain-source current (I_{DSS}) and cut-off frequency (f_T) for the MSAG process. ■

ACKNOWLEDGMENT

The author wishes to acknowledge the support of M/A-COM's layout, test, standard microwave products and wafer-processing groups in the successful development of the above MMICs.

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